REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-7 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the remarks as set forth below.

Rejection Under 35 U.S.C. § 102

Claim 1 stands rejected under 35 U.S.C. § 102 as being anticipated by Chang et al. (U.S. Patent No. 6,469,560). This rejection is respectfully traversed.

The Examiner states that Chang et al. teaches an electrostatic discharge protective circuit having a resistor device R1 with one end connected to a power supply, a capacitor device C1 which is connected in series between the resistor device and ground and a PMOS device P2 with a gate electrode connected between the resistor device and the capacitor device, the bulk electrode being interconnected to the first electrode and the first electrode connected to the power supply. Applicants submit that claim 1 is not anticipated by this reference.

Figure 4 of the present application shows an example of the present claimed invention with resistor 41, capacitor 42 and PMOS device 43. The first electrode 432 of the PMOS is connected directly to the power supply V_{cc}. This arrangement differs from the protective circuit disclosed by Chang et al. Chang et al. shows in Figure 4, protective circuit 100 including PMOS P2 connected between node A and node C. Resistor R2 is placed between node A and power source V_{cc}. Thus, resistor R2 is connected between the source/drain region of the PMOS and the power source so that the source/drain region

does not directly connect to the power source. This resistor is essential for the operation of the protective circuit in Chang.

During normal operation, the voltage at node B is equal to the power source voltage as discussed in column 4, lines 35 - 47, so that the PMOS is turned off. However, during an ESD event, the voltage at node A rises because of resistor R2 and the parasitic capacity. Because node B is at zero voltage and PMOS is turned on, the voltage at node C will increase to be that at node A when a stable state is reached. Thus, PMOS P2 merely functions as a switch to make the gate voltages of the two NMOS's 64 and 66 approximately equal during an ESD event. If resistor R2 is not present, both of the voltages at node A and node C will always be the low level whether PMOS P2 is turned on or not.

It is further pointed out that there is a parasitic diode existing in the PMOS, as shown in Figure 7 of the present application. In the Chang et al. device, because the voltage at node A is always higher than that at node C, the parasitic diode is ineffectual. However, this parasitic diode is useful in the present invention. Specifically, the PMOS shown in Figure 7 of the present invention is used to connect V_{cc2} with the voltage of the bus 63. During normal operation, since V_{cc2} is higher than the bus voltage, the PMOS is turned off. During an EDS event, if the ESD current flows into the bus, it can be directed to V_{cc2} through the parasitic diode. If the ESD current flows into the bus, because the gate voltage of the PMOS is close to zero volts due to the RC time delay, the PMOS will be turned on, and the ESD current can be directed to the bus. Thus, since the PMOS functions not only as a switch but also to conduct the ESD current, the two electrodes should not be

connected to resistors in order to avoid decreasing the conductive efficiency. Thus, including a resistor R2, such as shown in Chang et al. reduces the function of the present invention. For these reasons, Applicants submit that claim 1 is not anticipated by Chang et al.

Rejection Under 35 U.S.C. § 103

Claims 3 and 5-7 stand rejected under 35 U.S.C. § 103 as being obvious over Chang et al. The Examiner states that Chang et al. shows the ESD device in a similar fashion to claim 1. The Examiner further states that it would have been obvious to connect the protection circuits to each of power sources and connect the second electrode of the protection circuits to a common potential. Applicants submit that claims 3 and 5-7 are not obvious over this reference.

First, Applicants submit that the description of the ESD device in Chang et al. does not meet the terms of the claim, as described above in regard to claim 1. The same description of this part of the device is included in claim 3, and accordingly, claim 3 is allowable for the same reasons. Further, claim 3 includes the connection of the protection circuits to one of multiple power supplies with the second electrodes being connected to a common ESD bus. These features are not shown in the Chang et al. reference. Applicants submit that the addition of these features to Chang et al. would not be obvious to one having ordinary skill in the art, without some motivation for explaining why such a change should be made.

Furthermore, in the present invention, the ESD current can be directed to either electrode of the PMOS so the ESD protective circuit can be applied to a multi-power integrated circuit. As shown in Figure 6 of the present invention, during an ESD event, if the ESD current flows into V_{cc1}, it will be corrected to the common ESD bus by turning on the PMOS and it will then be directed to V_{cc2}, through the parasitic diode of PMOS 623. On the other hand, if the ESD current flows into V_{cc2}, it will be connected to V_{cc1} through a similar mechanism. However, the ESD protective circuit of Chang et al. is not suitable for a multi-power integrated circuit since the PMOS merely functions as a switch. Accordingly, Applicants submit that claim 3 would not be obvious over this reference.

Claims 5-7 depend from claim 3 and as such are also considered to be allowable. In addition, these claims further recite the voltages of the power supplies and the lack of current in the bus. Accordingly, these claims are believed to be additionally allowable.

Claims 2 and 4 stand rejected under 35 U.S.C. § 103 as being obvious over Chang et al. in view of Mentzer (U.S. Patent No.5,535,086). The Examiner relies on Mentzer to teach the RC time constant and states that it would have been obvious to one having ordinary skill in the art to utilize such a constant. Applicants submit that even if the Mentzer reference does teach this feature, that these claims are still allowable based on their dependency from allowable claims 1 and 3.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse (Reg. No. 27,295) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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